

## CLAIMS

1. An apparatus comprising/

a first delay circuit configured to present a data delayed signal having one of a plurality of delay times, wherein said plurality of delay times provide a user configurable setup/hold time.

2. The apparatus / according to claim 1, further comprising:

a second circuit configured to receive said data delayed signal and present a data output.

3. The apparatus according to claim 2, wherein said second circuit comprises a register that is further configured in response to a clock signal.

4. The apparatus according to claim 1, wherein said first delay circuit further comprises an HSTL circuit configured to present a first signal in response to a data input.

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5. The apparatus according to claim 4, wherein said first delay circuit further comprises one or more delay circuits each configured to present an output delay signal in response to said first signal.

6. The apparatus according to claim 5, wherein said first delay circuit further comprises a switch configured to receive said one or more output delay signals and present said data delayed signal.

7. The apparatus according to claim 6, wherein said switch is further configured in response to a user configuration signal.

8. The apparatus according to claim 7, wherein said user configuration signal comprises a setup and hold timing configuration signal.

9. The apparatus according to claim 7, wherein said user configuration signal comprises a programmable signal.

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10. The apparatus according to claim 7, wherein said user configuration signal comprises a multi-bit signal.

11. An apparatus comprising:

means for receiving an input signal; and

means for presenting a data delayed signal having one of a plurality of delay times to provide a user configurable setup/hold time.

12. A method for programming a data delayed signal, comprising the steps of:

(A) receiving an input signal; and

(B) configuring said data delayed signal having a plurality of delay times to provide a user configurable setup/hold time.

13. The method according to claim 12, further comprising the steps of:

(C) storing said data delayed signal and presenting a data output signal.

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Sub A3 14. The method according to claim 13, wherein step (C) is further configured in response to a clock signal.

15. The method according to claim 12, wherein step (B) further comprises presenting a first signal in response to said input signal.

16. The method according to claim 15, wherein step (B) further comprises presenting one or more output delay signals in response to said first signal.

17. The method according to claim 16, wherein step (B) further comprises receiving said one or more output delay signals and presenting said data delayed signal.

18. The method according to claim 17, wherein step (B) further comprises switching said one or more output delays in response to a user configuration signal.

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19. The method according to claim 18, wherein said user configuration signal comprises either (i) a setup and hold timing configuration signal or (ii) a multi-bit signal.

20. The method according to claim 18, wherein said user configuration signal comprises a programmable signal.

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